ABSTRACT OF THE DISCLOSURE Self-aligned Planar Double-Gate Process

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4 A double-gate transistor has front (upper) and back gates aligned laterally by a process of forming symmetric sidewalls in proximity to the front gate and 5 then oxidizing the back gate electrode at a temperature of at least 1000 6 7 degrees for a time sufficient to relieve stress in the structure, the oxide penetrating from the side of the transistor body to thicken the back gate 8 9 oxide on the outer edges, leaving an effective thickness of gate oxide at the center, aligned with the front gate electrode. Optionally, an angled implant 10 from the sides of an oxide enhancing species encourages relatively thicker 11 12 oxide in the outer implanted areas and an oxide-retarding implant across the transistor body retards oxidation in the vertical direction, thereby permitting 13 14 increase of the lateral extent of the oxidation

by Self-aligned Oxidation